IN THE CLAIMS

1 (Currently Amended). ~~A method~~ The method of claim 3 further comprising:

forming a metal oxide semiconductor field effect transistor having an epitaxially deposited source/drain that extends under the edges of a gate electrode.

2 (Original). The method of claim 1 including forming a source/drain extension that extends under the edges of a gate electrode.

3 (Currently Amended). ~~The method of claim 1 including~~ A method comprising:

forming a sacrificial epitaxially deposited material over a substrate; ~~and~~

forming a gate electrode over said epitaxially deposited layer; and

selectively etching said epitaxially deposited material.

4 (Original). The method of claim 3 wherein forming a sacrificial epitaxially deposited material includes epitaxially depositing a silicon material.

Claim 5 (Canceled).

6 (Original). The method of claim 5 including using sonication to selectively etch said material.

7 (Original). The method of claim 3 including forming a sidewall spacer on said gate electrode and etching under said sidewall spacer.

8 (Original). The method of claim 5 including selectively etching said epitaxially deposited material so as to undercut said gate electrode.

9 (Original). The method of claim 8 including depositing an epitaxial material on said substrate and extending under said gate electrode.

10 (Original). The method of claim 9 including forming a doped epitaxial material.

11 (Original). The method of claim 8 including forming said epitaxial material to be thinner near the gate electrode and thicker spaced from said gate electrode.

12 (Original). The method of claim 1 including forming a delta doped transistor.

Claims 13-19 (Canceled).

20 (Original). A method comprising:

forming a epitaxial semiconductor layer over a semiconductor substrate wherein the epitaxial semiconductor layer has a lower doping concentration than the substrate;

forming a gate structure including a gate electrode and a sidewall spacer over said epitaxial semiconductor layer; and

selectively etching the exposed portion of said epitaxial semiconductor layer as well as a portion of said epitaxial semiconductor layer under said gate electrode.

21 (Original). The method of claim 20 including epitaxially depositing a doped semiconductor material over said substrate to fill the region under said gate electrode and under said sidewall spacer.

22 (Original). The method of claim 21 wherein said epitaxial semiconductor layer has a first thickness under said gate electrode and a second thickness spaced from said gate electrode.

23 (Original). The method of claim 22 including forming said second thickness in alignment with said spacer.

24 (Original). The method of claim 20 including forming a deep source/drain region by ion implantation.

25 (Original). The method of claim 20 including forming said epitaxial semiconductor layer extending under said gate electrode and having a greater thickness outbound of said gate electrode and a lesser thickness under said gate electrode.

26 (New). A field effect transistor comprising:

a substrate;

a doped first epitaxial semiconductor material over said substrate;

a doped second epitaxial semiconductor material over said substrate;

said first and second epitaxial semiconductor materials being different materials; and

a gate electrode on said doped first and second epitaxial semiconductor material.

27 (New). The transistor of claim 26 including a source/drain having a source/drain extension, said source/drain extension being formed of said doped second epitaxial semiconductor material and extends under the edges of the gate electrode.

28 (New). The transistor of claim 27 wherein said second epitaxial semiconductor material has a first thickness near said gate electrode and a second thickness spaced from said gate electrode, said second thickness being greater than said first thickness.

29 (New). The transistor of claim 28 including a sidewall spacer, said material extending under said sidewall spacer.

30 (New). The transistor of claim 29 wherein said second thickness is aligned with said sidewall spacer.

31 (New). The transistor of claim 26 wherein said transistor is a delta doped transistor.

32 (New). The transistor of claim 26 including an ion implanted source/drain under said doped second epitaxial semiconductor material.